

# Linus Torvalds: AMD Intel's x86 tiers are 'garbage' and 'need to be eliminated'

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Linus Torvalds, the father of Linux, is perhaps one of the most controversial and outspoken tech moguls around. Torvalds' views are often described as 'rough but true', and almost always become a very interesting topic of discussion whether you agree with them or not.

When discussing the changes and additions to the new Linux KConfig (kernel configuration) build, Torvalds expressed his annoyance and apparent dissatisfaction with the AMD64 or x86\_64 architectural feature levels. He said:

On second thought, we shouldn't go into the x86-64 microarchitecture level. 'Cause this is silly stuff"

The whole "v2", "v3", "v4" etc levels seem crazy, stupid and need to be removed.

They have nothing to do with anything. Please \*don't\* put that crap in the kernel source.

I don't know who came up with this "micro-architecture level" crap, but as far as I know, it's completely informal and a buggy model.

There is a very real model for microarchitectural features and that is the CPUID bits. Trying to linearize those bits is technically wrong, because these things simply do not have a linear progression.

And worse, it's supposed to be a "simplification" but in fact adds complexity. Now instead of asking "Does this CPU support cmpxchg16?", the question becomes "What does 'v3' mean again?".

No. We \*NOT\* put that stupidity in the kernel.

Linus

For those who don't know, these x86-64 microarchitecture levels were introduced by Red Hat engineer Florian Weimer in 2020. Initially, "Levels A, B, and C" were proposed, and later "Level D" was added.

Essentially, these levels are in place to categorize CPU features in a chronological/time-ordered manner with the aim of simplifying the improvement of compatibility and coordination between hardware and operating

system/software through better compilation optimizations:

1. **x86-64-v2** supports vector instructions up to Streaming SIMD Extensions 4.2 (SSE4.2) and Supplemental Streaming SIMD Extensions 3 (SSSE3), the POPCNT instruction (useful for data analysis and bit-fiddling in some data structures), and CMPXCHG16B (a two-word compare-and-swap instruction useful for concurrent algorithms).
2. **x86-64-v3** adds vector instructions up to AVX2, MOVBE (for accessing big-endian data), and additional bitwise instructions.
3. **x86-64-v4** includes vector instructions from some AVX-512 variants.

Linus Torvalds felt that these architectural levels complicated things rather than simplified the problem, as linearizing the progression of hardware instructions and features was not a practical approach.



Torvalds' point here is valid because we often see certain CPU instructions, such as AVX, that can exist in some processor families but then disappear. A recent example is Intel introducing AVX-512 in the 11th generation Rocket Lake and then removing it in subsequent generations.

It's worth noting here that Linus Torvalds is now a prominent figure at the newly formed x86 Ecosystem Advisory Group, so his input is certainly valuable.

What do you think about the above opinion? Please leave a comment.

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