

Learn about HyperTransport technology

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Network Management - In this article we will introduce you to a solution to avoid affecting system performance related to data transmission capabilities.

Introduce

If you do a statistic you will find that after the 18-month period, the microprocessor's performance is approximately doubled. It is combined with multi-core technologies that make data transmission higher. This data transmission needs to occur between input and output devices (I / O), memory and between processors. Research in many computers today shows that data transmission capability is sometimes a limiting factor for overall system performance. Therefore, in this article, we will discuss a solution to fix that problem.

The solution for the higher data transfer referred to in this article is HyperTransport. Most users will recognize it from AMD products. In fact, HyperTransport is intended by AMD (to assist some partners in this area) although it is now managed and promoted by an independent group called the HyperTransport Consortium.

HyperTransport is a point-to-point connection system that focuses on chip-to-chip communication. From the beginning, it was designed to allow high-speed data transmission and low latency. One thing is essential in today's communication and in the future when the speed of CPU is increasing. Besides Chip-to-chip communication requires low latency and high performance.

Point-to-point technology, in contrast to the bus system, offers many advantages for chip-to-chip communication. One of the advantages is that communication signals do not require multiplex transmission. Besides, these communication signals also avoid interference and noise issues, which can be transmitted at low power levels. All that combined is for faster and clearer data transmission.

Another advantage of point-to-point technology is that it does not have to suffer from performance degradation like the PCI Buses suffer, the cause of which is the increase in the number of connected devices. HyperTransport only uses one direct connection between the two devices. That's why performance is guaranteed when multiple devices are connected.

Data package

HyperTransport is based on data packets. This type of transmission allows HyperTransport to perform a connection role for many different purposes. This technology can be used to connect processor cores, RAM and CPU, or even external memory devices. Since it is a packet-based transport form, the connected hardware forms a bearing. In that case, if a super-computer has a network of processors connected with point-to-point

technology, it is very beneficial.

Overhead of low package

Like most networks, HyperTransport networks also have performance characteristics. HyperTransport shows very high indicators when compared to other connection technologies such as PCI Express. One reason for that is that the amount of data on its overhead is very small.

HyperTransport requires an 8 byte read control packet for read operations. For write operations, HyperTransport uses an 8 byte write control packet and a 4 byte read response packet. That's all the data in its overhead; 8 bytes for read operation, 12 bytes for write operation. Meanwhile PCI Express requires 20 to 24 bytes of overhead for its read and write operations. This has answered HyperTransport's higher performance reasons.

But all is not perfect, so is HyperTransport. We need to appreciate the PCI Express technology here. With HyperTransport, the packet follows control packets with only 4 to 64 bytes. Meanwhile, data packets for PCI Express can be up to 4096 bytes. Therefore, in some cases, PCI Express can give performance using overhead over lower data transfer than HyperTransport. However, in case your read and write operations only require small data packets, using HyperTransport will bring significant performance to you.

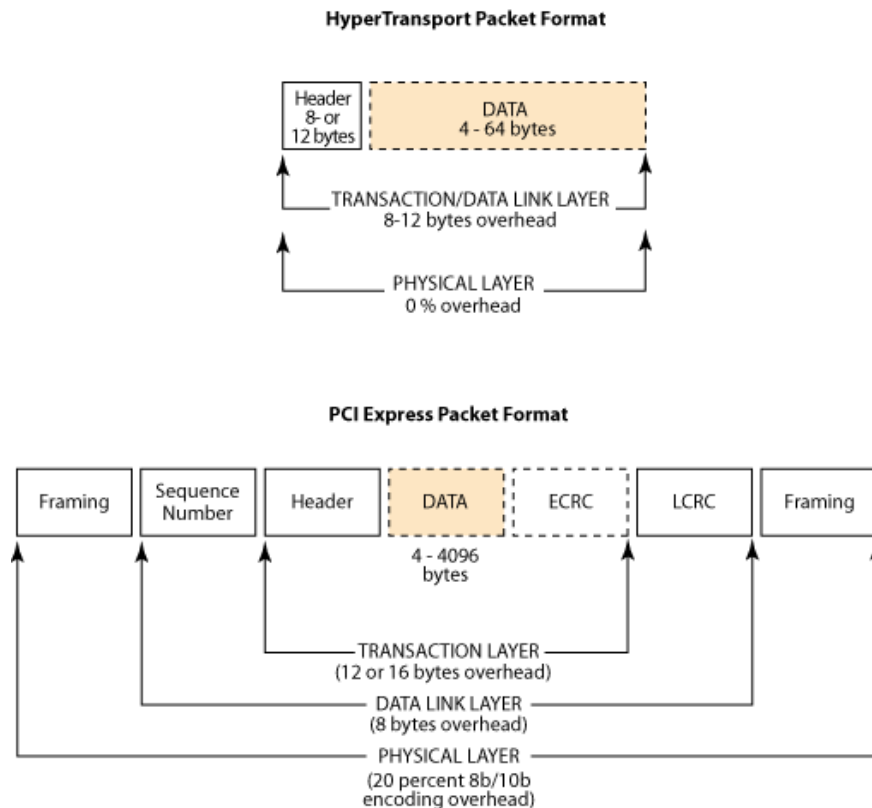


Figure 1: Diagram of overhead of HyperTransport and PCI Express

Bandwidth

Initially HyperTransport was designed to provide higher bandwidth performance than other competing technologies. One way it does so is to provide Double Data Rate (DDR). Normally, when digital data is

transmitted between two points, it will be read with highs or lows corresponding to 1 or 0. This data is read whenever the clock generates a high signal. With DDR feature, data can be read at both the rising and falling edges of the clock signal. That means that in a clock cycle, data can be read twice, thereby doubling the data transfer rate.

Low latency

Low latency is a design parameter focused on HyperTransport technology right from the start. HyperTransport can achieve this by adding a clock signal line in a set of 8 data bit paths. This performance is very significant compared to other technologies such as PCI Express, PCI Express technology that only has clocks embedded in an encryption scheme and decrypts complexly at both ends of a data link. The method used HyperTransport shows a reduction in latency when compared to other technologies because the device transmitting data does not need to be time-consuming for clock coding and receiving devices without the need to spend time on clock decoding.

Insert priority request

Another aspect that helps HyperTransport increase its performance is Priority Request Interleaving (PRI). This is a fairly new idea and brings many effects. Figure 2 below shows how PRI works. The problem that PRI solves here is: When the CPU is in a long communication chain with peripheral B, while A's peripheral needs to communicate with the CPU, normally device A will have to wait until when device B ends the communication process to switch to communication with it; however, this can take a long time and will obviously reduce the overall performance of the system.

PRI technology allows peripheral A to insert a PRI packet into the data stream of device B. This PRI packet is read by another CPU that can then initialize the communication chain with device A on one Other affiliate channels.

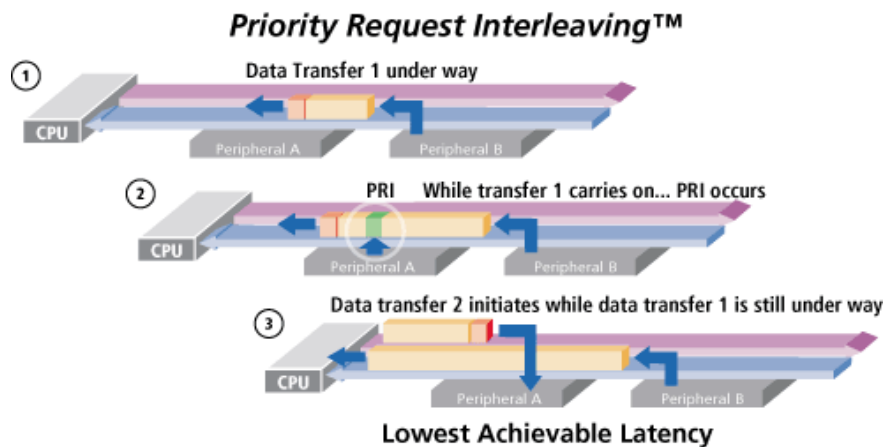


Figure 2: Diagram of PRI explanation.

HyperTransport technology has been designed from the outset to provide wide-ranging connectivity, enabling high communication speeds with low latency, high bandwidth, and high scalability. It can be said that the project has achieved its objectives. HyperTransport is used in many applications, from consumer electronics, home computers, enterprise-class networking devices, high-end networking equipment, and even supercomputers.

However, not all applications use HyperTransport technology in the same way. Some processors have true HyperTransport technology. Such processors are provided from AMD, Transmeta, Broadcom, and PMC Sierra. Some other processors only use HyperTransport as a high-performance bus to transmit data from PCI, PCI Express, USB and other technologies through the system.

Conclude

Although HyperTransport is an interesting technology with many performance advantages, we obviously cannot deny other technologies. Engineers need to carefully consider their needs carefully to choose which technology is suitable for a particular application. In the next section, we will introduce you in detail about some other connectivity technologies.

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